cannot be perfectly buried by the insulating layer. A void which extends long in the longitudinal direction of the transfer gate in a plan view often occurs in the insulating layer. Fig. 15 is a plan view showing arrangement of transfer gates and polypads in a DRAM (Dynamic Random Access Memory). Fig. 16 is a cross section taken along line XVI-XVI of Fig. 15. In Fig. 15, in an insulating interlayer 108 for burying the gap between two transfer gates 103, a region 109a with the high possibility of a void occurrence is extending along the gap. In Fig. 16, reference numeral 101 denotes a semiconductor substrate and reference numeral 103a denotes a nitride protection film. When a void 109 occurs in the region 109a as shown in Fig. 16, polysilicon enters the void at the time of depositing polysilicon for making a polypad, and a short circuit occurs between neighboring polypads 104a and 104b as shown in Fig. 17. In Fig. 17, polysilicon 114 for burying the void is deposited so as to connect the neighboring polypads 104a and 104b. When such a short circuit occurs, the product yield of manufacturing deteriorates. It might cause a delay in deliveries and the like.

REMARKS

Claims 1 through 11 are pending in this application, of which claims 1 through 6 stand withdrawn from consideration pursuant to the provisions of 37 C.F.R. §1.142(b). Accordingly, claims 7 through 11 are active.

The title and specification have been amended to address formalistic issues. Applicants submit that the present Amendment does not generate any new matter issue.